SPECIFICATION

TITLE OF THE INVENTION

Variable-frequency pulse generator

TECHNICAL FIELD

The present invention relates to a variable-frequency pulse generator capable of generating a pulse of the desired frequency.

BACKGROUND ART

A conventional variable-frequency pulse generator will be explained below. A conventional variable-frequency pulse generator has been disclosed in Japanese Patent Application No. 11-220364. Fig. 12 shows a configuration of a variable-frequency pulse generator disclosed in the above publication.

In Fig. 12, the reference symbol 100 denotes a conventional variable-frequency pulse generation circuit, 101 denotes a bit inverter which inverts a first reference value D1, 102 denotes a data selector which selects either one of the output of the inverter 101 and a pulse number set value Ps, 103 denotes a digital adder which adds the output θ1 of a first data holding circuit described later and the output of the data selector 102, and 104 denotes

the first data holding circuit which latches the output $\theta 2$ of the digital adder 103 at the timing T2 of a reference clock fb. The reference symbol 105 denotes a first data comparator which compares the output $\theta 1$ of the first data holding circuit 104 and the first reference value D1, and 106 denotes a second data comparator which compares the output $\theta 1$ of the first data holding circuit 104 and a second reference value D2. The reference symbol 107 denotes a pulse generation circuit which judges the output level (High or Low) based on the two comparison results, 108 denotes a second data holding circuit which latches the output fd of the pulse generation circuit 107 at the timing T3 of the reference clock fb and outputs a pulse train fout, and 109 denotes an overflow prevention circuit which outputs the overflow prevention signal fob synchronous with the reference clock fb based on the comparison result of the first data comparator 105.

The control clock frequency fc is [fb/4]. The first reference value D1 is [fc × n], and the second reference value D2 is [(fc/2) × n]. The pulse number set value per n seconds Ps is [Vp × n], and the value thereof can be set for 1 unit in the range of [0 ≤ Ps ≤ {(fc/2) × n}]. n denotes the maximum cycle of the output pulse, and Vp denotes a speed set value.

The operation of the conventional variable-frequency

pulse generator will now be explained. The inverter 101 outputs a bit inversion value of the reference value D1 in the 26-bit notation. When the S terminal is 0 ($\theta 1 \leq D1$), the data selector 102 outputs the pulse number set value Ps (26-bit notation) of a terminal A to a terminal Y, and when the S terminal is 1 ($\theta 1 > D1$), the data selector 102 outputs the bit inversion value of the reference value D1 of a terminal B to the terminal Y.

When a CIN terminal is 0 ($\theta 1 \leq D1$), the digital adder 103 adds the pulse number set value Ps output from the data selector 102 and the output $\theta 1$ of the first data holding circuit 104, and when the CIN terminal is 1 ($\theta 1 > D1$), the digital adder 103 adds $-(fc \times n)$, being the sum of the output of the data selector 102 and CIN = 1, and the output $\theta 1$ of the first data holding circuit 104, and outputs the addition result $\theta 2$ (26-bit notation) for each case. The first data holding circuit 104 latches the addition result $\theta 2$ at the timing T2 of the reference clock fb and the overflow prevention signal fob, and outputs data $\theta 1$ (26-bit notation).

The first data comparator 105 compares the output $\theta 1$ of the first data holding circuit 104 and the first reference value D1, and when $\theta 1 > D1$, outputs 1 as the overflow signal. The second data comparator 106 compares the output $\theta 1$ of the first data holding circuit 104 and the second reference value D2. The pulse generation circuit 107 judges the both

comparison results, and for example, when the comparison results by the both comparators are $0 \leq \theta 2 < D2$ (= $(fc/2) \times n$), outputs 0 as the judgment result fd, and when $D2 \leq \theta 2 < D1$ (= $fc \times n$), outputs 1, and when $D1 \leq \theta 2$, outputs 0. The second data holding circuit 108 latches the judgment result fd at the timing T3 of the reference clock fb, and outputs a pulse train fout.

The overflow prevention circuit 109 receives the overflow signal output from the first data comparator 105 at the timing T4 of the reference clock fb, and outputs an overflow prevention signal fob.

Fig. 13 is a timing chart which shows the operation of the conventional variable-frequency pulse generator. At first, the speed change timing Δt changes at a period synchronous with the timing T1 of the reference clock fb and the speed change timing, and acceleration and deceleration speed is latched at the timing T1 of the reference clock fb. This operation is executed by the part other than the configuration shown in Fig. 12.

The first data holding circuit 104 latches the output $\theta 2$ of the digital adder 103 at the timing T2 of the reference clock fb. The second data holding circuit 108 then latches the output fd of the pulse generation circuit 107 at the timing T3 of the reference clock fb, and outputs the pulse train fout.

The overflow prevention circuit 109 performs overflow prevention processing with respect to the output θ1 of the first data holding circuit 104, at the timing T4 of the reference clock fb. That is, when overflow occurs (θ1 > D1), and fb = (High), the overflow prevention circuit 109 outputs the overflow prevention signal fob (= High).

However, in the conventional variable-frequency pulse generator, control for four cycles of the reference clock is necessary during the period of from the speed setting until the overflow prevention processing is completed, that is, during 1 cycle of output control of the pulse train fout. Therefore, the reference clock of a frequency of 8 times or more is required in order to actually obtain the pulse train of a desired frequency (see Fig. 13). As a result, in the conventional variable-frequency pulse generator, with the speed-up of the reference clock, there is caused a problem in that the noise, power consumption and heat generation of the whole apparatus considerably increase.

It is an object of the present invention to provide a variable-frequency pulse generator capable of reducing the noise, power consumption and heat generation compared to the conventional apparatus.

DISCLOSURE OF THE INVENTION

The variable-frequency pulse generator according to

the present invention has a configuration such that one cycle of output control of the pulse train is executed by two cycles of the reference clock, and for example, comprises an inversion unit (corresponding to an inverter 11 in the embodiment described later) which inverts a first reference value regulated by the reference clock, a selection unit (corresponding to a data selector 12) which selects the first reference value after inversion, when an overflow has occurred, and in any other event selects a predetermined value which changes depending on a set speed, a data holding unit (corresponding to a first data holding circuit 14) which latches an output of a previous stage, being the present value of a result of addition, in the second cycle of the reference clock and at a predetermined timing of an overflow prevention signal, an addition unit (corresponding to a digital adder 13) which adds the value selected by the selection unit and the data latched by the data holding unit, a first comparison unit (corresponding to a first data comparator 15) which compares the value obtained by the addition unit as a result of addition and the first reference value, a second comparison unit (corresponding to a second data comparator 16) which compares the value obtained by the addition unit as a result of addition and a second reference value which is half of the first reference value, a judgment unit (corresponding to a pulse generation circuit

17) which judges whether a condition "0 ≤ addition result < second reference value" is satisfied, or whether a condition "second reference value ≤ addition result < first reference value" is satisfied, or whether a condition "first reference value ≤ addition result" is satisfied, and outputs a specified signal corresponding to a result of the judgment, a pulse train output unit (corresponding to a second data holding circuit 18) which latches the specified signal at a predetermined timing of the second cycle of the reference clock, and outputs a pulse train of a desired frequency, a third comparison unit (corresponding to a third data comparator 19) which compares the data latched by the data holding unit and the first reference value, and when a condition "latched data ≥ first reference value" is satisfied, judges that the overflow has occurred, and an overflow prevention unit (corresponding to an overflow prevention circuit 20) which outputs the overflow prevention signal at a predetermined timing of the first cycle of the reference clock, when the third comparison unit has judged that the overflow has occurred.

The variable-frequency pulse generator according to the next invention has a configuration such that one cycle of output control of the pulse train is executed by two cycles of the reference clock, and for example, comprises an addition unit (corresponding to a digital adder 21) which

adds a predetermined value, which changes depending on a set speed, and data latched at a predetermined timing of the second cycle of the reference clock, a subtraction unit (corresponding to a digital subtracter 22) which subtracts a first reference value regulated by the reference clock from the value obtained by the addition unit as a result of addition, a first comparison unit (corresponding to a first data comparator 25) which compares the value obtained by the addition unit as a result of addition and the first reference value, and when a condition "addition result ≥ first reference value" is satisfied, judges that an overflow has occurred, a second comparison unit (corresponding to a second data comparator 26) which compares the value obtained by the addition unit as a result of addition and a second reference value which is half of the first reference value, a selection unit (corresponding to a data selector 23) which selects the value obtained by the subtraction unit as a result of subtraction when the overflow has occurred, and in any other event selects the value obtained by the addition unit as a result of addition, a data holding unit (corresponding to a first data holding circuit 24) which latches the value selected by the selection unit at a predetermined timing of the second cycle of the reference clock, a judgment unit (corresponding to a pulse generation circuit 27) which judges based on each the results of

comparisons in the first comparison unit and the second comparison unit, whether a condition " 0 ≤ addition result < second reference value" is satisfied, or whether a condition "second reference value ≤ addition result < first reference value" is satisfied, or whether a condition "first reference value ≤ addition result" is satisfied, and outputs a specified signal according to a result of the judgment, and a pulse train output unit (corresponding to a second data holding circuit 28) which latches the specified signal at a predetermined timing of the second cycle of the reference clock, and outputs a pulse train of a desired frequency.

The variable-frequency pulse generator according to the next invention has a configuration such that one cycle of output control of the pulse train is executed by two cycles of the reference clock, and for example, comprises an inversion unit which inverts a reference value regulated by the reference clock, a selection unit which selects the reference value after inversion, when an overflow has occurred, and in any other event selects a predetermined value which changes depending on a set speed, a data holding unit which latches an output of a previous stage, being the present value of a result of addition, in the second cycle of the reference clock and at a predetermined timing of an overflow prevention signal, an addition unit which adds the value selected by the selection unit and the data latched

by the data holding unit, a first comparison unit which compares the value obtained by the addition unit as a result of addition and the reference value, a judgment unit (corresponding to a pulse generation circuit 17c) which judges whether a condition "the overflow frequency is an even number" and "0 ≤ addition result < reference value" is satisfied, or whether a condition "the overflow frequency is an even number" and "reference value ≤ addition result" is satisfied, or whether conditions "the overflow frequency is an odd number" and "0 ≤ addition result < reference value" are satisfied, or whether conditions "the overflow frequency is an odd number" and "reference value ≤ addition result" are satisfied, and outputs a specified signal corresponding to a result of the judgment, a pulse train output unit which latches the specified signal at a predetermined timing of the second cycle of the reference clock, and outputs a pulse train of a desired frequency, a second comparison unit which compares the data latched by the data holding unit and the reference value, and when a condition "latched data ≥ reference value" is satisfied, judges that the overflow has occurred, and an overflow prevention unit which outputs the overflow prevention signal at a predetermined timing of the first cycle of the reference clock, when the second comparison unit has judged that the overflow has occurred.

The variable-frequency pulse generator according to

the next invention has a configuration such that one cycle of output control of the pulse train is executed by two cycles of the reference clock, and for example, comprises an inversion unit which inverts a first reference value regulated by the reference clock, a selection unit which selects the first reference value after inversion, when an overflow has occurred, and in any other event selects a predetermined value which changes depending on a set speed, a data holding unit which latches an output of a previous stage, being the present value of a result of addition, in the second cycle of the reference clock and at a predetermined timing of the overflow prevention signal, an addition unit which adds the value selected by the selection unit and the data latched by the data holding unit, a first comparison unit which compares the value obtained by the addition unit as a result of addition and the first reference value, a second comparison unit which compares the value obtained by the addition unit as a result of addition and a second reference value which is half of the first reference value, a judgment unit which judges whether a condition "0 ≤ addition result < second reference value" is satisfied, or whether a condition "second reference value ≤ addition result < first reference value" is satisfied, or whether a condition "first reference value ≤ addition result < (second reference value × 3)" is satisfied, or whether a condition "(second reference

value × 3) ≤ addition result" is satisfied, and outputs a specified signal corresponding to a result of the judgment, a pulse train output unit which latches the specified signal at a predetermined timing of the second cycle of the reference clock, and outputs a pulse train of a desired frequency, a third comparison unit (corresponding to a third data comparator 19d) which compares the data latched by the data holding unit and the first reference value, and when a condition "latched data > first reference value" is satisfied, judges that the overflow has occurred, and an overflow prevention unit which outputs the overflow prevention signal at a predetermined timing of the first cycle of the reference clock, when the third comparison unit has judged that the overflow has occurred.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the configuration of a first embodiment of a variable-frequency pulse generator according to the present invention, Fig. 2 is a timing chart which shows the operation of the variable-frequency pulse generator in the first embodiment, Fig. 3 shows the output result of each section, when the variable-frequency pulse generator in the first embodiment is operated, Fig. 4 shows the output waveform of the variable-frequency pulse generator in the first embodiment, Fig. 5 shows the configuration of a second

embodiment of the variable-frequency pulse generator according to the present invention, Fig. 6 is a timing chart which shows the operation of the variable-frequency pulse generator in the second embodiment, Fig. 7 shows the output result of each section, when the variable-frequency pulse generator in the second embodiment is operated, Fig. 8 shows the configuration of a third embodiment of the variable-frequency pulse generator according to the present invention, Fig. 9 shows the output result of each section, when the variable-frequency pulse generator in the third embodiment is operated, Fig. 10 shows the configuration of a fourth embodiment of the variable-frequency pulse generator according to the present invention, Fig. 11 shows the output result of each section, when the variable-frequency pulse generator in the fourth embodiment is operated, Fig. 12 shows the configuration of a conventional variable-frequency pulse generator, and Fig. 13 is a timing chart which shows the operation of the conventional variable-frequency pulse generator.

BEST MODE FOR CARRYING OUT THE INVENTION

Embodiments of the variable-frequency pulse generator according to this invention will be explained in detail below with reference to the accompanying drawings. However, this invention is not limited by these embodiments.

First Embodiment:

Fig. 1 shows the configuration of a first embodiment of the variable-frequency pulse generator according to the present invention. In Fig. 1, the reference symbol 1a denotes a variable-frequency pulse generation circuit in the first embodiment, 11 denotes a bit inverter which inverts a first reference value D1, 12 denotes a data selector which selects either one of the output of the inverter 11 and a pulse number set value Ps, 13 denotes a digital adder which adds the output θ1 of a first data holding circuit 14 described later and the output of the data selector 12, and 14 denotes a first data holding circuit which latches the output θ2 of the digital adder 13 at the timing T2 of a reference clock fb. The reference symbol 15 denotes a first data comparator which compares the output θ2 of the digital adder 13 and the first reference value D1, and 16 denotes a second data comparator which compares the output θ2 of the digital adder 13 and a second reference value D2. The reference symbol 17 denotes a pulse generation circuit which judges the output level (High or Low) based on the two comparison results, 18 denotes a second data holding circuit which latches the output fd of the pulse generation circuit 17 at the timing T2 of the reference clock fb and outputs a pulse train fout, 19 denotes a third data comparator which compares the output θ1 of the first data holding circuit 14 and the first reference

value D1, and 20 denotes an overflow prevention circuit which outputs an overflow prevention signal fob based on the comparison result of the third data comparator 19.

In the first embodiment, the control clock frequency fc is [fb/2], and the first reference value D1 is [fc × n], and the second reference value D2 is [(fc/2) × n]. The pulse number set value per n seconds Ps is [Vp × n], and the value thereof can be set per one unit in the range of [$0 \leq Ps \leq \{(fc/2) \times n\}$]. However, n denotes the maximum cycle of the output pulse, and Vp denotes a speed set value.

In the first embodiment, as one example, explanation is given by assuming that the reference clock frequency fb is 32 MHz, and the maximum cycle n of the output pulse is 2 seconds. In this case, the control clock frequency fc becomes fc = fb/2 = 32 MHz/2 = 16 MHz, the first reference value D1 becomes D1 = fc × n = 16 MHz × 2 = 32 M, the second reference value D2 becomes D2 = (fc/2) × n = (16 MHz/2) × 2 = 16 M, and the pulse number set value per n seconds (hereinafter referred to as a "pulse number set value") Ps becomes $0 \leq Ps \leq 16$ MHz. Therefore, the speed set value Vp becomes $0 \leq Vp \leq 8$ MHz.

The operation of the variable-frequency pulse generator in the first embodiment will now be explained. The inverter 11 outputs a bit inversion value of the reference value D1 in the 26-bit notation. When the S terminal is

0 ($\theta 1 < D1$), the data selector 12 outputs the pulse number set value Ps (26-bit notation) of a terminal A to a terminal Y, and when the S terminal is 1 ($\theta 1 \geq D1$), the data selector 12 outputs the bit inversion value of the reference value D1 of a terminal B to the terminal Y.

When the CIN terminal is 0 ($\theta 1 < D1$), the digital adder 13 adds the pulse number set value Ps output from the data selector 12 and the output $\theta 1$ of the first data holding circuit 14, and when the CIN terminal is 1 ($\theta 1 \geq D1$), the digital adder 13 adds $-(fc \times n)$, being the sum of the output of the data selector 12 and CIN = 1, and the output $\theta 1$ of the first data holding circuit 14, and outputs the addition result $\theta 2$ (26-bit notation) for each case. The first data holding circuit 14 latches the addition result $\theta 2$ at the timing T2 of the reference clock fb and the overflow prevention signal fob, and outputs data $\theta 1$ (26-bit notation).

The first data comparator 15 compares the output $\theta 2$ of the digital adder 13 and the first reference value D1. The second data comparator 16 compares the output $\theta 2$ of the digital adder 13 and the second reference value D2. The pulse generation circuit 17 judges the both comparison results, and for example, when the comparison results by the both comparators are $0 \leq \theta 2 < D2$ $(= (fc/2) \times n)$, outputs 0 as the judgment result fd, and when $D2 \leq \theta 2 < D1$ $(= fc \times n)$, outputs 1, and when $D1 \leq \theta 2$, outputs 0. The second

data holding circuit 18 latches the judgment result fd at the timing T2 of the reference clock fb, and outputs a pulse train fout.

The third data comparator 19 compares the output θ1 of the first data holding circuit 14 and the first reference value D1, and when $\theta 1 < D1$, outputs 0, and when $\theta 1 \geq D1$, outputs 1. The overflow prevention circuit 20 receives the output of the third data comparator 19 at the timing T1 of the reference clock fb, and outputs an overflow prevention signal fob.

Fig. 2 is a timing chart which shows the operation of the variable-frequency pulse generator in the first embodiment. At first, the speed change timing Δt changes at a period synchronous with the timing T1 of the reference clock fb and the speed change timing, and acceleration and deceleration speed is latched at the timing T1 of the reference clock fb. This operation is executed by the part other than the configuration shown in Fig. 1.

The first data holding circuit 14 latches the output θ2 of the digital adder 103 at the timing T2 of the reference clock fb. The second data holding circuit 18 then latches the output fd of the pulse generation circuit 17, and outputs the pulse train fout.

The overflow prevention circuit 20 performs overflow prevention processing with respect to the output θ1 of the

first data holding circuit 14, at the timing T1 of the reference clock fb. That is, when overflow occurs ($\theta 1 \geq D1$, and fb = High), the overflow prevention circuit 20 outputs the overflow prevention signal fob (= High). In the first embodiment, the above processing is repetitively executed at timings T1 and T2 of the reference clock fb.

Fig. 3 shows the output result of each section, when the variable-frequency pulse generator in the first embodiment is operated. Here, it is assumed that the reference clock fb is 32 MHz, the maximum cycle n of the output pulse is 2 seconds, and the pulse number set value Ps is 8 → 16 MHz (that is, the speed set value Vp is set to 4 → 8 MHz). Therefore, the control clock frequency fc becomes 16 MHz, the first reference value D1 becomes 32 M, and the second reference value D2 becomes 16 M.

In Fig. 3, for example, at the point of time when the elapsed time is 0 second (initial state: 0/32 MHz), either of the pulse number set value Ps (Vp × n), the output value $\theta 1$ of the first data holding circuit 14, the overflow signal, the output value $\theta 2$ of the digital adder 13, the value fd, and the value fout is 0 (initial value).

When the elapsed time is 1/32 MHz (at the timing T1 of fb), the pulse number set value Ps is Vp × n = 4 MHz × 2 = 8 MHz, and the first data holding circuit 14 holds the previous (elapsed time = 0 second) output value $\theta 1$ (= 0).

The third data comparator 19 outputs 0 ($\theta 1 < D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 0 + 8$ MHz = 8 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 0, since $0 \leq \theta 2 < D2$, and the output value fout of the second data holding circuit 18 holds the previous fout value, and fout = 0.

When the elapsed time is 2/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 1/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1$ = 8 MHz. The third data comparator 19 outputs 0 ($\theta 1 < D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps$ = 8 MHz + 8 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 18 latches the value fd (= 0) immediately before and the output value fout thereof becomes fout = 0.

When the elapsed time is 3/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 holds the previous (elapsed time = 2/32 MHz) output value $\theta 1$ (= 8 MHz). The third data comparator 19 outputs

0 ($\theta 1 < D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 8$ MHz + 8 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 18 holds the previous value fout (= 0) and the output value fout thereof becomes fout = 0.

When the elapsed time is 4/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 3/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1 = 16$ MHz. The third data comparator 19 outputs 0 ($\theta 1 < D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 16$ MHz + 8 MHz = 24 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

When the elapsed time is 5/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 14 holds the previous (elapsed time = 4/32 MHz) output value $\theta 1$ (= 16 MHz). The third data comparator 19 outputs

0 ($\theta1 < D1$) as the overflow signal. The output value $\theta2$ of the digital adder 13 is $\theta2 = \theta1 + Ps = 16$ MHz + 8 MHz = 24 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 1, since $D2 \leq \theta2 < D1$, and the second data holding circuit 18 holds the previous value fout (= 1) and the output value fout thereof becomes fout = 1.

When the elapsed time is 6/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta2$ immediately before (elapsed time = 5/32 MHz) and the output value $\theta1$ thereof becomes $\theta1 = 24$ MHz. The third data comparator 19 outputs 0 ($\theta1 < D1$) as the overflow signal. The output value $\theta2$ of the digital adder 13 is $\theta2 = \theta1 + Ps = 24$ MHz + 8 MHz = 32 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 0, since $D1 \leq \theta2$, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

When the elapsed time is 7/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 14 holds the previous (elapsed time = 6/32 MHz) output value $\theta1$ (= 24 MHz). The third data comparator 19 outputs

0 ($\theta 1 < D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 24$ MHz + 8 MHz = 32 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 0, since $D2 \leq \theta 2$, and the second data holding circuit 18 holds the previous value fout (= 1) and the output value fout thereof becomes fout = 1.

When the elapsed time is 8/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 7/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1$ = 32 MHz. The third data comparator 19 outputs 1 ($\theta 1 \geq D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 - D1$ = 32 MHz-32 MHz = 0 MHz, since the overflow signal is 1. The output value fd of the pulse generation circuit 17 is fd = 0, since $0 \leq \theta 2 < D2$, and the second data holding circuit 18 latches the value fd (= 0) immediately before and the output value fout thereof becomes fout = 0.

When the elapsed time is 9/32 MHz (at the timing T1 of fb), the pulse number set value Ps is changed to $Vp \times n$ = 16 MHz, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 8/32 MHz), and the output value $\theta 1$ thereof becomes $\theta 1$ = 0 MHz.

The third data comparator 19 outputs 0 ($\theta 1 < D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 0$ MHz + 16 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 18 holds the previous value fout (= 0) and the output value fout thereof becomes fout = 0.

When the elapsed time is 10/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n$ = 16 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 9/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1$ = 16 MHz. The third data comparator 19 outputs 0 ($\theta 1 < D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps$ = 16 MHz + 16 MHz = 32 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17 is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

Hereinafter, the similar operation is performed for the elapsed time 11/32 MHz and the elapsed time 12/32 MHz, ..., and the output as shown in Fig. 3 can be obtained.

Fig. 4 shows the output waveform of the variable-frequency pulse generator in the first embodiment.

In the variable-frequency pulse generator, during the elapsed time of from 0 to 8 [unit of 31.25 ns], that is, during $31.25 \times 8 = 250$ ns, the speed set value is Vp = 4 MHz, and the output pulse fout becomes also 4 MHz, and it is seen that the pulse is output as per the speed set value Vp. On the other hand, during the elapsed time of from 8 to 16 [unit of 31.25 ns], that is, during $31.25 \times 8 = 250$ ns, the speed set value is Vp = 8 MHz, and the output pulse fout becomes also 8 MHz, and it is also seen that the pulse is output as per the speed set value Vp. In this manner, in the variable-frequency pulse generator in the first embodiment, the output pulse changes corresponding to the change in the speed set value.

As described above, in the first embodiment, one cycle of the output control of the pulse train fout is changed from four cycles (T1-T4) to two cycles (T1-T2) of the reference clock, by comparing the output θ2 of the digital adder 13 before being held by the first data holding circuit 14, and the first reference value D1 and the second reference value D2, respectively, by the first data comparator 15 and the second data comparator 16. The latch timing of the overflow signal is also changed from T4 to T1 of the reference clock fb, by comparing the output θ1 of the first data holding circuit 14 and the first reference value D1 by the third data comparator 19. Thereby, the control cycle can be

reduced, and the noise, power consumption and heat generation can be reduced, compared to the conventional art.

Second Embodiment:

Fig. 5 shows the configuration of a second embodiment of the variable-frequency pulse generator according to the present invention. In Fig. 5, the reference symbol 1b denotes a variable-frequency pulse generation circuit in the second embodiment, 21 denotes a digital adder which adds the output θ1 of a first data holding circuit 24 described later and the pulse number set value Ps, and 22 denotes a digital subtracter which subtracts a first reference value D1 from the output θ2 of the digital adder 21. The reference symbol 23 denotes a data selector which selects either one of the output of the output θ2 of the digital adder 21 and the output θ3 of the digital subtracter 22, 24 denotes a first data holding circuit which latches the output of the data selector 23 at the timing T2 of the reference clock fb, 25 denotes a first data comparator which compares the output θ2 of the digital adder 21 and the first reference value D1, and 26 denotes a second data comparator which compares the output θ2 of the digital adder 21 and the second reference value D2. The reference symbol 27 denotes a pulse generation circuit which judges the output level (High or Low) based on the two comparison results, and 28 denotes a second data holding circuit which latches the output fd

of the pulse generation circuit 27 at the timing T2 of the reference clock fb and outputs a pulse train fout.

In the second embodiment, the control clock frequency fc is [fb/2]. The first reference value D1 is [fc × n], and the second reference value D2 is [(fc/2) × n]. The pulse number set value per n seconds Ps is [Vp × n], and the value thereof can be set per one unit in the range of [$0 \le Ps \le \{(fc/2) \times n\}$]. n denotes the maximum cycle of the output pulse, and Vp denotes a speed set value.

In the second embodiment, as one example, explanation is given by assuming that the reference clock frequency fb is 32 MHz, and the maximum cycle n of the output pulse is 2 seconds. In this case, the control clock frequency fc becomes fc = fb/2 = 32 MHz/2 = 16 MHz, the first reference value D1 becomes D1 = fc × n = 16 MHz × 2 = 32 M, the second reference value D2 becomes D2 = (fc/2) × n = (16 MHz/2) × 2 = 16 M, and the pulse number set value per n seconds (hereinafter referred to as a "pulse number set value") Ps becomes $0 \le Ps \le 16$ MHz. Therefore, the speed set value Vp becomes $0 \le Vp \le 8$ MHz.

The operation of the variable-frequency pulse generator in the second embodiment will now be explained. The digital adder 21 adds the pulse number set value Ps (26-bit notation) and the output θ1 of the first data holding circuit 24 (26-bit notation), and outputs the addition result θ2

(26-bit notation). However, $0 \leq \theta 2 < ((fc/2) \times n + fc \times n)$. The digital subtracter 22 subtracts the first reference value D1 from the output θ2 of the digital adder 21, and outputs the subtraction result θ3 (26-bit notation). However, $-(fc \times n) \leq \theta 3 < ((fc/2) \times n)$.

When the S terminal is 1 ($\theta 2 < D1$), the data selector 23 outputs the data θ2 of the terminal B to the terminal Y, and when the S terminal is 0 ($\theta 2 \geq D1$), the data selector 23 outputs the data θ3 of the terminal A to the terminal Y. The first data holding circuit 24 latches the output of the data selector 23 at the timing T2 of the reference clock fb, and outputs data θ1 (26-bit notation). However, $0 \leq \theta 1 < (fc \times n)$.

The first data comparator 25 compares the output θ2 of the digital adder 21 and the first reference value D1. The second data comparator 26 compares the output θ2 of the digital adder 13 and the second reference value D2. The pulse generation circuit 27 judges the both comparison results, and for example, when the comparison results by the both comparators are $0 \leq \theta 2 < D2$ ($= (fc/2) \times n$), outputs 0 as the judgment result fd, and when $D2 \leq \theta 2 < D1$ ($= fc \times n$), outputs 1, and when $D1 \leq \theta 2$, outputs 0. The second data holding circuit 28 latches the judgment result fd at the timing T2 of the reference clock fb, and outputs a pulse train fout.

Fig. 6 is a timing chart which shows the operation of the variable-frequency pulse generator in the second embodiment. At first, the speed change timing Δt changes at a period synchronous with the timing T1 of the reference clock fb and the speed change timing, and acceleration and deceleration speed is latched at the timing T1 of the reference clock fb. This operation is executed by the part other than the configuration shown in Fig. 5.

The first data holding circuit 24 latches the output of the data selector 23 at the timing T2 of the reference clock fb. The second data holding circuit 28 then latches the output fd of the pulse generation circuit 27, and outputs the pulse train fout.

Fig. 7 shows the output result of each section, when the variable-frequency pulse generator in the second embodiment is operated. Here, it is assumed that the reference clock fb is 32 MHz, the maximum cycle n of the output pulse is 2 seconds, and the pulse number set value Ps is 8 → 16 MHz (that is, the speed set value Vp is set to 4 → 8 MHz). Therefore, the control clock frequency fc becomes 16 MHz, the first reference value D1 becomes 32 M, and the second reference value D2 becomes 16 M.

In Fig. 7, for example, at the point of time when the elapsed time is 0 second (initial state: 0/32 MHz), either of the pulse number set value Ps (Vp × n), the output value

$\theta 1$ of the first data holding circuit 24, the output value $\theta 2$ of the digital adder 21, the output value $\theta 3$ of the digital subtracter 22, the value of Pin, the value fd, and the value fout is 0 (initial value).

When the elapsed time is 1/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n = 4$ MHz $\times 2 = 8$ MHz, and the first data holding circuit 24 holds the previous (elapsed time = 0 second) output value $\theta 1$ (= 0). The output value $\theta 2$ of the digital adder 21 is $\theta 2 = \theta 1 + Ps = 0 + 8$ MHz = 8 MHz, and output value $\theta 3$ of the digital subtracter 22 is $\theta 3 = \theta 2 - D1 = 8$ MHz-32 MHz = -24 MHz. At this time, the output Pin of the data selector 23 becomes $\theta 2$. The output value fd of the pulse generation circuit 27 is fd = 0, since $0 \leq \theta 2 < D2$, and the output value fout of the second data holding circuit 28 holds the previous fout value, and fout = 0.

When the elapsed time is 2/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 24 latches the output value Pin = $\theta 2$ immediately before (elapsed time = 1/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1 = 8$ MHz. The output value $\theta 2$ of the digital adder 21 is $\theta 2 = \theta 1 + Ps = 8$ MHz + 8 MHz = 16 MHz, and the output value $\theta 3$ of the digital subtracter 22 is $\theta 3 = \theta 2 - D1 = 16$ MHz-32 MHz = -16 MHz. At this time, the output Pin

of the data selector 23 becomes $\theta 2$. The output value fd of the pulse generation circuit 27 is fd = 1, since $D2 \le \theta 2 < D1$, and the second data holding circuit 28 latches the value fd (= 0) immediately before and the output value fout thereof becomes fout = 0.

When the elapsed time is 3/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n = 4$ MHz $\times$ 2 = 8 MHz, and the first data holding circuit 24 holds the previous (elapsed time = 2/32 MHz) output value $\theta 1$ (= 8 MHz). The output value $\theta 2$ of the digital adder 21 is $\theta 2 = \theta 1 +$ Ps = 8 MHz + 8 MHz = 16 MHz, and the output value $\theta 3$ of the digital subtracter 22 is $\theta 3 = \theta 2 - D1$ = 16 MHz-32 MHz = -16 MHz. At this time, the output Pin of the data selector 23 becomes $\theta 2$. The output value fd of the pulse generation circuit 27 is fd = 1, since $D2 \le \theta 2 < D1$, and the second data holding circuit 28 holds the previous value fout and the output value fout thereof becomes fout = 0.

When the elapsed time is 4/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 24 latches the output value Pin = $\theta 2$ immediately before (elapsed time = 3/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1$ = 16 MHz. The output value $\theta 2$ of the digital adder 21 is $\theta 2 = \theta 1$ + Ps = 16 MHz + 8 MHz = 24 MHz, and the output value $\theta 3$ of the digital subtracter 22 is $\theta 3$

$= \theta 2 - D1 = 24$ MHz-32 MHz $= -8$ MHz. At this time, the output Pin of the data selector 23 becomes $\theta 2$. The output value fd of the pulse generation circuit 27 is fd = 1, since $D2 \le \theta 2 < D1$, and the second data holding circuit 28 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

When the elapsed time is 5/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n = 4$ MHz $\times 2 = 8$ MHz, and the first data holding circuit 24 holds the previous (elapsed time = 4/32 MHz) output value $\theta 1$ (= 16 MHz). The output value $\theta 2$ of the digital adder 21 is $\theta 2 = \theta 1 + Ps = 16$ MHz $+ 8$ MHz $= 24$ MHz, and the output value $\theta 3$ of the digital subtracter 22 is $\theta 3 = \theta 2 - D1 = 24$ MHz-32 MHz$=-8$ MHz. At this time, the output Pin of the data selector 23 becomes $\theta 2$. The output value fd of the pulse generation circuit 27 is fd = 1, since $D2 \le \theta 2 < D1$, and the second data holding circuit 28 holds the previous value fout and the output value fout thereof becomes fout = 1.

When the elapsed time is 6/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 24 latches the output value Pin = $\theta 2$ immediately before (elapsed time = 5/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1 = 24$ MHz. The output value $\theta 2$ of the digital adder 21 is $\theta 2 = \theta 1 + Ps = 24$ MHz $+ 8$ MHz $= 32$ MHz,

and the output value $\theta 3$ of the digital subtracter 22 is $\theta 3 = \theta 2 - D1$ = 32 MHz-32 MHz = 0 MHz. At this time, the output Pin of the data selector 23 becomes $\theta 3$. The output value fd of the pulse generation circuit 27 is fd = 0, since $D1 \leq \theta 2$, and the second data holding circuit 28 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

When the elapsed time is 7/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n$ = 4 MHz × 2 = 8 MHz, and the first data holding circuit 24 holds the previous (elapsed time = 6/32 MHz) output value $\theta 1$ (= 24 MHz). The output value $\theta 2$ of the digital adder 21 is $\theta 2 = \theta 1 + Ps$ = 24 MHz + 8 MHz = 32 MHz, and the output value $\theta 3$ of the digital subtracter 22 is $\theta 3 = \theta 2 - D1$ = 32 MHz-32 MHz = 0 MHz. At this time, the output Pin of the data selector 23 becomes $\theta 3$. The output value fd of the pulse generation circuit 27 is fd = 0, since $D2 \leq \theta 2$, and the second data holding circuit 28 holds the previous value fout and the output value fout thereof becomes fout = 1.

When the elapsed time is 8/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 24 latches the output value Pin = $\theta 3$ immediately before (elapsed time = 7/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1$ = 0 MHz. The output value $\theta 2$ of the digital

adder 21 is $\theta 2 = \theta 1 + Ps = 0$ MHz + 8 MHz = 8 MHz, and the output value $\theta 3$ of the digital subtracter 22 is $\theta 3 = \theta 2 - D1$ = 8 MHz-32 MHz = -24 MHz. At this time, the output Pin of the data selector 23 becomes $\theta 2$. The output value fd of the pulse generation circuit 27 is fd = 0, since $0 \leq \theta 2 < D2$, and the second data holding circuit 28 latches the value fd (= 0) immediately before and the output value fout thereof becomes fout = 0.

When the elapsed time is 9/32 MHz (at the timing T1 of fb), the pulse number set value Ps is changed to Vp × n = 16 MHz, and the first data holding circuit 24 holds the previous (elapsed time = 8/32 MHz) output value $\theta 1$ (= 0 MHz). The output value $\theta 2$ of the digital adder 21 is $\theta 2 = \theta 1 + Ps = 0$ MHz + 16 MHz = 16 MHz, and the output value $\theta 3$ of the digital subtracter 22 is $\theta 3 = \theta 2 - D1$ = 16 MHz-32 MHz = -16 MHz. At this time, the output Pin of the data selector 23 becomes $\theta 2$. The output value fd of the pulse generation circuit 27 is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 28 holds the previous value fout and the output value fout thereof becomes fout = 0.

When the elapsed time is 10/32 MHz (at the timing T2 of fb), the pulse number set value Ps is Vp × n = 16 MHz similar to the previous elapsed time, and the first data holding circuit 24 latches the output value Pin = $\theta 2$ immediately before (elapsed time = 9/32 MHz) and the output

value $\theta1$ thereof becomes $\theta1$ = 16 MHz. The output value $\theta2$ of the digital adder 21 is $\theta2 = \theta1 + Ps$ = 16 MHz + 16 MHz = 32 MHz, and the output value $\theta3$ of the digital subtracter 22 is $\theta3 = \theta2-D1$ = 32 MHz-32 MHz = 0 MHz. At this time, the output Pin of the data selector 23 becomes $\theta3$. The output value fd of the pulse generation circuit 27 is fd = 0, since $D1 \leq \theta2$, and the second data holding circuit 28 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

Hereinafter, similar operation is performed for the elapsed time 11/32 MHz and the elapsed time 12/32 MHz, ..., and the output as shown in Fig. 7 can be obtained. The output waveform of the variable-frequency pulse generator in the second embodiment changes corresponding to the change in the speed set value, as in Fig. 4 explained above.

As described above, in the second embodiment, one cycle of the output control of the pulse train fout is changed from four cycles (T1-T4) to two cycles (T1-T2) of the reference clock, by comparing the output $\theta2$ of the digital adder 21 before being held by the first data holding circuit 24, and the first reference value D1 and the second reference value D2, respectively, by the first data comparator 25 and the second data comparator 26. The digital subtracter 22 further subtracts the first reference value D1 from the output $\theta2$ of the digital adder 21, and when the comparison

result by the first data comparator 25 satisfies $\theta 2 \geq D1$, the data selector 23 selects and outputs $\theta 3$, being the subtraction result, to thereby prevent the overflow of the digital adder 21. Thereby, the control cycle can be reduced, and the noise, power consumption and heat generation can be reduced, compared to the conventional art.

Third Embodiment:

Fig. 8 shows the configuration of a third embodiment of the variable-frequency pulse generator according to the present invention. The same configuration as that of the first embodiment described above is denoted by the same reference symbol, and the explanation thereof is omitted. Only the operation different from that of the first embodiment will be explained herein.

In Fig. 8, the reference symbol 1c is a variable-frequency pulse generation circuit in the third embodiment, and 17c is a pulse generation circuit which judges the output level (High or Low) based on the comparison result of the second data comparator 16. As in the first embodiment, the control clock frequency fc is [fb/2], and the second reference value D2 is [(fc/2) × n]. In the second embodiment, as one example, explanation is given by assuming that the reference clock frequency fb is 32 MHz, and the maximum cycle n of the output pulse is 2 seconds.

The operation of the variable-frequency pulse

generator in the third embodiment will be explained. The inverter 11 outputs a bit inversion value of the reference value D2 in the 25-bit notation. When the S terminal is 0 ($\theta1 < D1$), the data selector 12 outputs the pulse number set value Ps (25-bit notation) of the terminal A to the terminal Y, and when the S terminal is 1 ($\theta1 \geq D2$), the data selector 12 outputs the bit inversion value of the reference value D2 of the terminal B to the terminal Y.

When the CIN terminal is 0 ($\theta1 < D2$), the digital adder 13 adds the pulse number set value Ps output from the data selector 12 and the output θ1 of the first data holding circuit 14, and when the CIN terminal is 1 ($\theta1 \geq D2$), the digital adder 13 adds $-(fc/2 \times n)$, being the sum of the output of the data selector 12 and CIN = 1, and the output θ1 of the first data holding circuit 14, and outputs the addition result θ2 (25-bit notation) for each case. The first data holding circuit 14 latches the addition result θ2 at the timing T2 of the reference clock fb and the overflow prevention signal fob, and outputs data θ1 (25-bit notation).

The second data comparator 16 compares the output θ2 of the digital adder 13 and the second reference value D2. The pulse generation circuit 17c judges the comparison result of the second data comparator 16, and for example, when the comparison result is $0 \leq \theta2 < D2$ ($= (fc/2) \times n$) and the overflow is even number of times, outputs 0 as the judgment result

fd, and when $D2 \leq \theta2$ and the overflow is even number of times, outputs 1, and when $0 \leq \theta2 < D2$ ($= (fc/2) \times n$) and the overflow is odd number of times, outputs 1, and when $D2 \leq \theta2$ and the overflow is odd number of times, outputs 0. The second data holding circuit 18 latches the judgment result fd at the timing T2 of the reference clock fb, and outputs a pulse train fout.

The third data comparator 19 compares the output $\theta1$ of the first data holding circuit 14 and the second reference value D2, and when $\theta1 < D2$, outputs 0, and when $\theta1 \geq D2$, outputs 1. The overflow prevention circuit 20 receives the output of the third data comparator 19 at the timing T1 of the reference clock fb, and outputs an overflow prevention signal fob.

The latch timing of the variable-frequency pulse generator in the third embodiment is the same as that shown in Fig. 2 explained above, and hence the explanation thereof is omitted.

Fig. 9 shows the output result of each section, when the variable-frequency pulse generator in the third embodiment is operated. It is assumed that the reference clock fb is 32 MHz, the maximum cycle n of the output pulse is 2 seconds, and the pulse number set value Ps is 8 $\rightarrow$ 16 MHz (that is, the speed set value Vp is set to 4 $\rightarrow$ 8 MHz). Therefore, the control clock frequency fc becomes 16 MHz,

and the second reference value D2 becomes 16 M.

In Fig. 9, for example, at the point of time when the elapsed time is 0 second (initial state: 0/32 MHz), either of the pulse number set value Ps (Vp × n), the output value θ1 of the first data holding circuit 14, the overflow signal, the output value θ2 of the digital adder 13, the value fd, and the value fout is 0 (initial value).

When the elapsed time is 1/32 MHz (at the timing T1 of fb), the pulse number set value Ps is Vp × n = 4 MHz × 2 = 8 MHz, and the first data holding circuit 14 holds the previous (elapsed time = 0 second) output value θ1 (= 0). The third data comparator 19 outputs 0 (θ1 < D2) as the overflow signal. The output value θ2 of the digital adder 13 is θ2 = θ1 + Ps = 0 + 8 MHz = 8 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17c is fd = 0, since the overflow frequency is 0 (0 is designated as an even number) 0 ≤ θ2 < D2, and the output value fout of the second data holding circuit 18 holds the previous fout value, and fout = 0.

When the elapsed time is 2/32 MHz (at the timing T2 of fb), the pulse number set value Ps is Vp × n = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value θ2 immediately before (elapsed time = 1/32 MHz) and the output value θ1 thereof becomes θ1 = 8 MHz. The third data comparator 19 outputs

0 ($\theta 1 < D2$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 8$ MHz + 8 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17c is fd = 1, since the overflow frequency is 0 and $D2 \leq \theta 2$, and the second data holding circuit 18 latches the value fd (= 0) immediately before and the output value fout thereof becomes fout = 0.

When the elapsed time is 3/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 14 holds the previous (elapsed time = 2/32 MHz) output value $\theta 1$ (= 8 MHz). The third data comparator 19 outputs 0 ($\theta 1 < D2$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 8$ MHz + 8 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17c is fd = 1, since the overflow frequency is 0 and $D2 \leq \theta 2$, and the second data holding circuit 18 holds the previous value fout (= 0) and the output value fout thereof becomes fout = 0.

When the elapsed time is 4/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 3/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1 = 16$ MHz. The third data comparator 19 outputs

1 ($\theta 1 \geq D2$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 - D2$ = 16 MHz-16 MHz = 0 MHz, since the overflow signal is 1. The output value fd of the pulse generation circuit 17c is fd = 1, since the overflow frequency is 1 and $0 \leq \theta 2 < D2$, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

When the elapsed time is 5/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 4/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1$ = 0 MHz. The third data comparator 19 outputs 0 ($\theta 1 < D2$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps$ = 0 MHz + 8 MHz = 8 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17c is fd = 1, since the overflow frequency is 1 and $0 \leq \theta 2 < D2$, and the second data holding circuit 18 holds the previous value fout (= 1) and the output value fout thereof becomes fout = 1.

When the elapsed time is 6/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 5/32 MHz) and the output value $\theta 1$ thereof

becomes $\theta 1$ = 8 MHz. The third data comparator 19 outputs 0 ($\theta 1 < D2$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps$ = 8 MHz + 8 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17c is fd = 0, since the overflow frequency is 1 and $D2 \leq \theta 2$, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

When the elapsed time is 7/32 MHz (at the timing T1 of fb), the pulse number set value Ps is Vp × n = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 holds the previous (elapsed time = 6/32 MHz) output value $\theta 1$ (= 8 MHz). The third data comparator 19 outputs 0 ($\theta 1 < D2$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps$ = 8 MHz + 8 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17c is fd = 0, since the overflow frequency is 1 and $D2 \leq \theta 2$, and the second data holding circuit 18 holds the previous value fout (= 1) and the output value fout thereof becomes fout = 1.

When the elapsed time is 8/32 MHz (at the timing T2 of fb), the pulse number set value Ps is Vp × n = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 7/32 MHz) and the output value $\theta 1$ thereof

becomes $\theta 1 = 16$ MHz. The third data comparator 19 outputs 1 ($\theta 1 \geq D2$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 - D2 = 16$ MHz-16 MHz $= 0$ MHz, since the overflow signal is 1. The output value fd of the pulse generation circuit 17c is fd = 0, since the overflow frequency is 2 and $0 \leq \theta 2 < D2$, and the second data holding circuit 18 latches the value fd (= 0) immediately before and the output value fout thereof becomes fout = 0.

When the elapsed time is 9/32 MHz (at the timing T1 of fb), the pulse number set value Ps is changed to $Vp \times n = 16$ MHz, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 8/32 MHz) and the output value $\theta 1$ becomes $\theta 1 = 0$ MHz. The third data comparator 19 outputs 0 ($\theta 1 < D2$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 0$ MHz $+ 16$ MHz $= 16$ MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17c is fd = 1, since the overflow frequency is 2 and $D2 \leq \theta 2$, and the second data holding circuit 18 holds the previous value fout (= 0) and the output value fout thereof becomes fout = 0.

When the elapsed time is 10/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n = 16$ MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately

before (elapsed time = 9/32 MHz) and the output value θ1 thereof becomes θ1 = 16 MHz. The third data comparator 19 outputs 1 (θ1 ≥ D2) as the overflow signal. The output value θ2 of the digital adder 13 is θ2 = θ1-D2 = 16 MHz-16 MHz = 0 MHz, since the overflow signal is 1. The output value fd of the pulse generation circuit 17c is fd = 1, since the overflow frequency is 3 and 0 ≤ θ2 < D1, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

Hereinafter, similar operation is performed for the elapsed time 11/32 MHz and the elapsed time 12/32 MHz, ..., and the output as shown in Fig. 9 can be obtained. The output waveform of the variable-frequency pulse generator in the third embodiment changes corresponding to the change in the speed set value, as in Fig. 4 explained above.

As described above, in the third embodiment, one cycle of the output control of the pulse train fout is changed from four cycles (T1-T4) to two cycles (T1-T2) of the reference clock, by comparing the output θ2 of the digital adder 13 before being held by the first data holding circuit 14, and the second reference value D2, respectively, by the second data comparator 16. The latch timing of the overflow signal is also changed from T4 to T1 of the reference clock fb, by comparing the output θ1 of the first data holding circuit 14 and the second reference value D2 by the third

data comparator 19. Thereby, the control cycle can be reduced, and the noise, power consumption and heat generation can be reduced, compared to the conventional art.

Also, in the third embodiment, it is judged whether the overflow frequency is an even number of times or an odd number of times, and the pulses are generated based on the judgment result and the comparison result by the second data comparator 16. Thereby, the number of gates can be reduced than that in the first embodiment.

Fourth Embodiment:

Fig. 10 shows the configuration of a fourth embodiment of the variable-frequency pulse generator according to the present invention. The same configuration as that of the first embodiment described above is denoted by the same reference symbol, and the explanation thereof is omitted. Only the operation different from that of the first embodiment will be explained herein.

In Fig. 10, the reference symbol 1d is a variable-frequency pulse generation circuit in the third embodiment, and 17d is a pulse generation circuit which judges the output level (High or Low) based on the comparison result of the two data comparators, and 19d is a third data comparator which compares the output θ1 of the first data holding circuit 14 and the first reference value D1. In the embodiment, as one example, explanation is given by

assuming that the reference clock frequency fb is 32 MHz, and the maximum cycle n of the output pulse is 2 seconds.

The operation of the variable-frequency pulse generator in the fourth embodiment will be explained. When the S terminal is 0 ($\theta 1 \leq D1$), the data selector 12 outputs the pulse number set value Ps (26-bit notation) of the terminal A to the terminal Y, and when the S terminal is 1 ($\theta 1 > D1$), the data selector 12 outputs the bit inversion value of the reference value D1 of the terminal B to the terminal Y.

When the CIN terminal is 0 ($\theta 1 \leq D1$), the digital adder 13 adds the pulse number set value Ps output from the data selector 12 and the output $\theta 1$ of the first data holding circuit 14, and when the CIN terminal is 1 ($\theta 1 > D1$), the digital adder 13 adds $-(fc \times n)$, being the sum of the output of the data selector 12 and CIN = 1, and the output $\theta 1$ of the first data holding circuit 14, and outputs the addition result $\theta 2$ (26-bit notation) for each case.

The pulse generation circuit 17d judges the comparison results of the first and second data comparators, and for example, when the comparison results by the both comparators are $0 \leq \theta 2 < D2$ ($= (fc/2) \times n$), outputs 0 as the judgment result fd, and when $D2 \leq \theta 2 < D1$ ($= fc \times n$), outputs 1, and when $D1 \leq \theta 2 < (D2 \times 3)$, outputs 0, and when $(D2 \times 3) \leq \theta 2$, outputs 1.

The third data comparator 19d compares the output $\theta 1$ of the first data holding circuit 14 and the first reference value D1, and when $\theta 1 \leq D1$, outputs 0, and when $\theta 1 > D1$, outputs 1.

The latch timing of the variable-frequency pulse generator in the fourth embodiment is the same as that shown in Fig. 2 explained above, and hence the explanation thereof is omitted.

Fig. 11 shows the output result of each section, when the variable-frequency pulse generator in the fourth embodiment is operated. It is assumed herein that the reference clock fb is 32 MHz, the maximum cycle n of the output pulse is 2 seconds, and the pulse number set value Ps is 8 $\rightarrow$ 16 MHz (that is, the speed set value Vp is set to 4 $\rightarrow$ 8 MHz). Therefore, the control clock frequency fc becomes 16 MHz, and the first reference value D1 becomes 32 MHz, and the second reference value D2 becomes 16 MHz.

In Fig. 11, for example, at the point of time when the elapsed time is 0 second (initial state: 0/32 MHz), either of the pulse number set value Ps (Vp $\times$ n), the output value $\theta 1$ of the first data holding circuit 14, the overflow signal, the output value $\theta 2$ of the digital adder 13, the value fd, and the value fout is 0 (initial value).

When the elapsed time is 1/32 MHz (at the timing T1 of fb), the pulse number set value Ps is Vp $\times$ n = 4 MHz $\times$

2 = 8 MHz, and the first data holding circuit 14 holds the previous (elapsed time = 0 second) output value θ1 (= 0). The third data comparator 19d outputs 0 ($\theta 1 \leq D1$) as the overflow signal. The output value θ2 of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 0 + 8$ MHz = 8 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17d is fd = 0, since $0 \leq \theta 2 < D2$, and the output value fout of the second data holding circuit 18 holds the previous fout value, and fout = 0.

When the elapsed time is 2/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value θ2 immediately before (elapsed time = 1/32 MHz) and the output value θ1 thereof becomes θ1 = 8 MHz. The third data comparator 19d outputs 0 ($\theta 1 \leq D1$) as the overflow signal. The output value θ2 of the digital adder 13 is $\theta 2 = \theta 1 + Ps$ = 8 MHz + 8 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17d is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 18 latches the value fd (= 0) immediately before and the output value fout thereof becomes fout = 0.

When the elapsed time is 3/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding

circuit 14 holds the previous (elapsed time = 2/32 MHz) output value $\theta 1$ (= 8 MHz). The third data comparator 19d outputs 0 ($\theta 1 \le D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 8$ MHz + 8 MHz = 16 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17d is fd = 1, since $D2 \le \theta 2 < D1$, and the second data holding circuit 18 holds the previous value fout (= 0) and the output value fout thereof becomes fout = 0.

When the elapsed time is 4/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 3/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1 = 16$ MHz. The third data comparator 19d outputs 0 ($\theta 1 \le D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 16$ MHz + 8 MHz = 24 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17d is fd = 1, since $D2 \le \theta 2 < D1$, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

When the elapsed time is 5/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n = 8$ MHz similar to the previous elapsed time, and the first data holding

circuit 14 holds the previous (elapsed time = 4/32 MHz) output value $\theta 1$ (= 16 MHz). The third data comparator 19d outputs 0 ($\theta 1 \leq D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 16$ MHz + 8 MHz = 24 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17d is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 18 holds the previous value fout (= 1) and the output value fout thereof becomes fout = 1.

When the elapsed time is 6/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value $\theta 2$ immediately before (elapsed time = 5/32 MHz) and the output value $\theta 1$ thereof becomes $\theta 1$ = 24 MHz. The third data comparator 19d outputs 0 ($\theta 1 \leq D1$) as the overflow signal. The output value $\theta 2$ of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 24$ MHz + 8 MHz = 32 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17d is fd = 0, since $D1 \leq \theta 2 < (D2 \times 3)$, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

When the elapsed time is 7/32 MHz (at the timing T1 of fb), the pulse number set value Ps is $Vp \times n$ = 8 MHz similar to the previous elapsed time, and the first data holding

circuit 14 holds the previous (elapsed time = 6/32 MHz) output value θ1 (= 24 MHz). The third data comparator 19d outputs 0 (θ1 ≤ D1) as the overflow signal. The output value θ2 of the digital adder 13 is θ2 = θ1 + Ps = 24 MHz + 8 MHz = 32 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17d is fd = 0, since D1 ≤ θ2 < (D2 × 3), and the second data holding circuit 18 holds the previous value fout (= 1) and the output value fout thereof becomes fout = 1.

When the elapsed time is 8/32 MHz (at the timing T2 of fb), the pulse number set value Ps is Vp × n = 8 MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value θ2 immediately before (elapsed time = 7/32 MHz) and the output value θ1 thereof becomes θ1 = 32 MHz. The third data comparator 19d outputs 0 (θ1 ≤ D1) as the overflow signal. The output value θ2 of the digital adder 13 is θ2 = θ1 + Ps = 32 MHz + 8 MHz = 40 MHz, since the overflow signal is 1. The output value fd of the pulse generation circuit 17d is fd = 0, since D1 ≤ θ2 < (D2 × 3), and the second data holding circuit 18 latches the value fd (= 0) immediately before and the output value fout thereof becomes fout = 0.

When the elapsed time is 9/32 MHz (at the timing T1 of fb), the pulse number set value Ps is changed to Vp × n = 16 MHz, and the first data holding circuit 14 holds the

previous (elapsed time = 8/32 MHz) output value θ1 (= 32 MHz). The third data comparator 19d outputs 0 ($\theta 1 \leq D1$) as the overflow signal. The output value θ2 of the digital adder 13 is $\theta 2 = \theta 1 + Ps = 32$ MHz + 16 MHz = 48 MHz, since the overflow signal is 0. The output value fd of the pulse generation circuit 17d is fd = 1, since $(D2 \times 3) \leq \theta 2$, and the second data holding circuit 18 holds the previous value fout (= 0) and the output value fout thereof becomes fout = 0.

When the elapsed time is 10/32 MHz (at the timing T2 of fb), the pulse number set value Ps is $Vp \times n = 16$ MHz similar to the previous elapsed time, and the first data holding circuit 14 latches the output value θ2 immediately before (elapsed time = 9/32 MHz) and the output value θ1 thereof becomes θ1 = 48 MHz. The third data comparator 19d outputs 1 ($\theta 1 > D1$) as the overflow signal. The output value θ2 of the digital adder 13 is $\theta 2 = \theta 1 - D1 = 48$ MHz-32 MHz = 16 MHz, since the overflow signal is 1. The output value fd of the pulse generation circuit 17d is fd = 1, since $D2 \leq \theta 2 < D1$, and the second data holding circuit 18 latches the value fd (= 1) immediately before and the output value fout thereof becomes fout = 1.

Hereinafter, similar operation is performed for the elapsed time 11/32 MHz and the elapsed time 12/32 MHz, ..., and the output as shown in Fig. 11 can be obtained. The

output waveform of the variable-frequency pulse generator in the fourth embodiment changes corresponding to the change in the speed set value, as in Fig. 4 explained above.

As described above, in the fourth embodiment, one cycle of the output control of the pulse train fout is changed from four cycles (T1-T4) to two cycles (T1-T2) of the reference clock, by comparing the output θ2 of the digital adder 13 before being held by the first data holding circuit 14, the first reference value D1 and the second reference value D2, respectively, by the first data comparator 15 and the second data comparator 16. The latch timing of the overflow signal is also changed from T4 to T1 of the reference clock fb. Thereby, the control cycle can be reduced, and the noise, power consumption and heat generation can be reduced, compared to the conventional art.

As described above, according to the present invention, the output of the addition unit before being held by the data holding unit, the first reference value and the second reference value are compared, respectively, by the first comparison unit and the second comparison unit, to thereby change one cycle of the output control of the pulse train from four cycles (T1-T4) to two cycles (T1-T2) of the reference clock. Further, by comparing the output of the data holding unit and the first reference value by the third comparison unit, the latch timing of the overflow signal

is changed from the fourth cycle (T4) to the first cycle (T1). Thereby, the control cycle can be reduced, and hence there is the effect that the noise, power consumption and heat generation can be reduced, compared to the conventional art.

According to the next invention, the output of the addition unit before being held by the data holding unit, the first reference value and the second reference value are compared, respectively, by the first comparison unit and the second comparison unit, to thereby change one cycle of the output control of the pulse train from four cycles (T1-T4) to two cycles (T1-T2) of the reference clock. Further, when the subtraction unit subtracts the first reference value from the output value of the addition unit, and the comparison result by the first comparison unit satisfies "addition result ≥ first reference value", the selection unit prevents the overflow of the addition unit by selecting/outputting the subtraction result. Thereby, the control cycle can be reduced, and hence there is the effect that the noise, power consumption and heat generation can be reduced, compared to the conventional art.

According to the next invention, it is judged whether the overflow frequency is even number of times or odd number of times, and the pulses are generated based on the judgment result and the comparison result by the second comparison

unit. Thereby, there is the effect that the number of gates can be considerably reduced.

According to the next invention, the output of the addition unit before being held by the data holding unit, the first reference value and the second reference value are compared, respectively, by the first comparison unit and the second comparison unit, to thereby change one cycle of the output control of the pulse train from four cycles (T1-T4) to two cycles (T1-T2) of the reference clock. Further, by comparing the output of the data holding unit and the first reference value by the third comparison unit, the latch timing of the overflow signal is changed from the fourth cycle (T4) to the first cycle (T1). Thereby, the control cycle can be reduced, and hence there is the effect that the noise, power consumption and heat generation can be reduced, compared to the conventional art.

INDUSTRIAL APPLICABILITY

As described above, the variable-frequency pulse generator according to the present invention is useful for a variable-frequency pulse generator which generates a pulse train of a desired frequency, and particularly useful for all apparatus which uses a variable-frequency pulse generator in which the noise, power consumption and heat generation within the apparatus considerably increase due

to speed-up of the reference block.